DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF ENGINEERING SCIENCE AND TECHNOLOGY,
SHIBPUR, HOWRAH-711 103.

No. 217/2021/EE-3/21(PS) Dated: 03/08/2021

From : The Head of the Department,
Electrical Engineering,
IIEST, Shibpur, Howrah-711 103

To : Enlisted vendors of the institute and other interested parties/ For Website Tender.

Dear Sir(s),

Sealed quotations are invited for supply of the following item(s) within **15 days** from the date of publication of this advertisement in the website. The quotation should include the 5% GST only as per institute rule, delivery charges, entry tax if any, etc. to The Head, Department of Electrical Engineering, Indian Institute of Engineering Science and Technology, Shibpur and should mention a firm delivery period. Preferences will be given to the suppliers who can supply ex-stock.

Any clarification regarding specification only can be obtained by sending e-mail to ps@ee.iiests.ac.in within 10 days after the publication of the advertisement in the website of the IIEST, Shibpur.

The vendors, who are not enlisted in the Institute register, should submit the copies of their valid Trade License, GST registration, PAN, latest Income Tax / Sales Tax Statement /Return, SSI/MSME certificate, if any etc. and any other commercial credentials. The institute will provide concessional GST rate certificate with the purchase order and will pay 5% GST only.

Yours faithfully,

Konika Das (Bhattacharya)

Please put your digital/scanned signature
Signature of the indenting Officer/
Concerned Faculty Member

Prof. & Head of EE Dept.
IIEST, Shibpur, Howrah – 711 103

Dr. Konika Das (Bhattacharya)
Professor & Head
Electrical Engineering Deptt.
Indian Institute of Engineering Science and Technology, Shibpur
Howrah-711 103

List of Items and the specifications:

As given in Annexure-1

Warranty requirement: 1 year warranty for the components used in the item

Note; Newspaper Advertisement should be considered as per Rules.
Konika Das (Bhattacharya)

Annexure-1

Converter Stack for Industrial Electronics Research Laboratory (IERL), EE Department, IIEST Shibpur

One set of Converter stack (power electronic converter system) is to be supplied as per the following specifications:

(1) The power circuit diagram for the converter system (indoor installation inside a laboratory environment with room temperature of about 40 deg C) to be integrated and supplied should be as per Fig. IERL_ZSI given below:

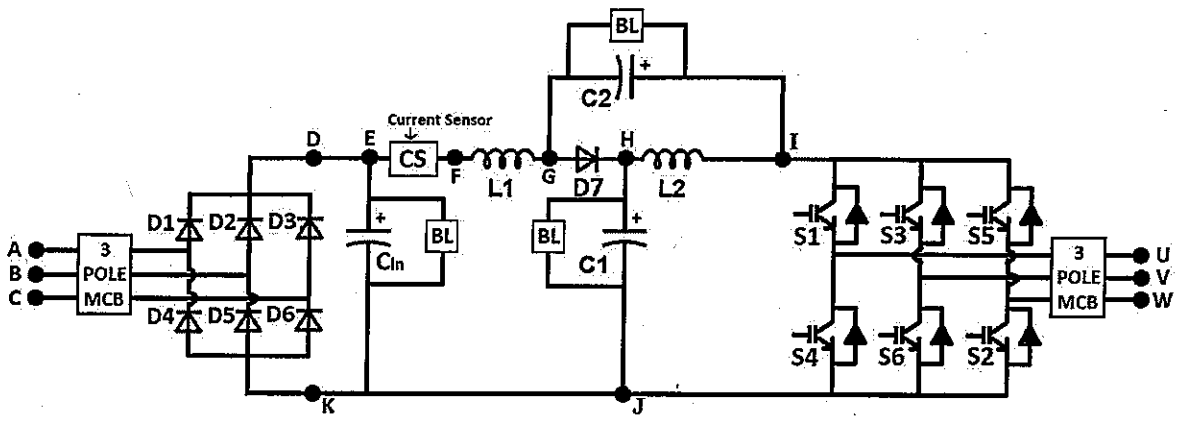

Fig. IERL_ZSI : Power circuit diagram of the converter stack (power converter system)

(2) The front-end three phase full-bridge diode rectifier system should have proper heat-sink mounted rectifier diodes (D1 TO D6 in Fig. IERL_ZSI), each having average current rating of 25A or above, reverse voltage rating of 800V or above. It should have proper snubbers connected.

(3) At the output of the front end three phase diode rectifier, a capacitor bank C_{in} (please see Fig. IERL_ZSI) should be provided, consisting of 2 no.s of PG-6DI grade electrolytic capacitors, each 1000 µF, 450V (rated voltage, 495V surge voltage rating) in parallel, along with 2 no. s of paralleled KP-3C series/equivalent high-frequency snubber capacitors, each of 0.56 µF, 1000V DC rating. A suitable bleeder resistor of around 33k, 10W rating should be provided across C_{in} as shown as the block BL in Fig. IERL_ZSI.

(4) Inductors as shown as L1 or L2 (please see Fig. IERL_ZSI) will be identical uncoupled DC inductors supplied to the vendor by the customer, i.e. IIEST Shibpur. These supplied inductors have to be assembled by the vendor inside the converter. Care must be taken that the magnetic flux created by one inductor should not influence the other inductor. Each will be ferrite core based with value of 20 mH with current ratings of 20A DC, 22A peak and capable of for carrying 20 kHz ripple currents of 2A rms. Class F or H insulation will be used, as applicable. Each inductor should be wrapped (shielded) by the vendor with thin aluminium sheets which should be eventually

equipment-earthed. A suitable clamp structure is to be built by the vendor to install each inductor inside the converter enclosure.

(5) Diode D7 (please see Fig. IERL_ZSI) should be an ultra-fast recovery diode or diode assembly capable of handling 30 kHz PWM ripple current having an average current rating of 25A or above and a reverse working voltage rating of 1700V or above.

(6) Capacitor bank shown as C1 (please see Fig. IERL_ZSI) should consist of an equivalent capacitance of Cornell Dubilier make/equivalent 140 μF, 1000V DC rated low-loss metallized polypropylene film capacitors with high frequency ripple current capability of at least 55A. A suitable high-value bleeder resistor should be provided across this capacitor assembly, C1, assuming that around 700V DC with 5% pk-to-pk ripple will appear across it.

(7) Capacitor bank shown as C2 (please see Fig. IERL_ZSI) should be same as bank C1. A suitable high-value bleeder resistor should be provided across this capacitor assembly, C1, assuming that around 750V DC with 5% pk-to-pk ripple will appear across it. Care must be taken that the electric field created by one capacitor should not influence the other capacitor.

(8) The 6 IGBT's, properly heat-sink mounted, each WITH an ANTIPARALLEL FREEWHEELING DIODE, marked as S1 to S6 (please see Fig. IERL_ZSI) should be each 75A or above, 1200V or above SEMIKRON or other reputed company MAKE devices/modules with suitable snubbers. These IGBTS should be one-leg modules and not discretes. Suitable SEMIKRON or other reputed company make galvanically/optically isolated drivers with their isolated regulated power supplies should be provided for these 6 IGBT's with at least 2 kV isolation level. The driver cards should allow for setting zero dead time between two switches of a single leg with either no 'desat' protection or 'desat' protection disabled. It is to be noted that two switches of a single leg will be deliberately shorted together for very short time durations by a suitable PWM control strategy operating with 15 kHz switching frequency to be used by the customer, while operating the converter system.

(9) Big blackened circles/nodes marked as A, B, C, D, E, F, G, H, I, J, K, U, V and W (please see Fig. IERL_ZSI) are terminals that should be brought out and terminated for customer's access. Terminals A, B, C, D and K should be 25A terminals; U, V, W should be 10A terminals and the other terminals should be 5A terminals.

(10) The block shown as CS (please see Fig. IERL_ZSI) should be a Hall-effect based current sensor, LEM 25NP or equivalent.

(11) A three-pole 25A, 415V C type Legrand/Siemens/L&T/equivalent MCB should be given at input as shown and a three-pole 6A, 415V C type Legrand/Siemens/equivalent MCB is to be provided as shown (please see Fig. IERL_ZSI).

(12) The customer will provide the vendor an FPGA (field programmable gates array) CARD assembly, consisting of two PCBs side by side connected with each other, having a combined size of 32 cm x 17 cm and this card assembly has to be mounted by the vendor inside the converter. The vendor has to provide a ± 15V, +1A/-1A regulated DC power supply and a +5V, +2A/-1A regulated DC power supply which will power up the FPGA card assembly. The customer must have an access to a power-up switch that should be installed to switch on and off these DC regulated power supplies. Detailed Schematics of the FPGA card will be ultimately supplied to the vendor. The FPGA card system has 8 ADC channels and 4 DAC channels and these terminals along with the analog ground terminal should have to be brought out by the vendor and terminated outside properly for customer's access. A 40 pin digital I/O, employing Texas

Instruments make SN74ALVC164245 3.3V-5V level shifting transceivers/buffers at the end-stage, form a part of the FPGA card assembly. Six of these 40 pins have to be utilized by the vendor and should be routed through a suitably-designed signal-conditioning card and interfaced as the input signals for the selected driver stages for the six IGBTs of the converter marked as S1, S2, S3, S4, S5 and S6 in Fig. IERL_ZSI. The remaining 34 digital I/O pins including the digital ground terminal should be brought out by the vendor and terminated outside for customer's access. This FPGA card will be programmed by the customer utilizing a PC (not within vendor's scope of supply) through a byteblaster communication cable and this cable will be provided by the customer to the vendor. The 'FPGA-end' of the byteblaster cable should be terminated by the vendor with the FPGA card inside the converter and the 'PC end' of the cable should be brought out by the vendor for giving the option to the customer to connect to a USB port of a PC.

(13)The whole converter setup should be forced air-cooled by a suitable fan with properly designed inlets/outlet vents.

(14)The converter should be housed inside a rugged enclosure with vents and earthing terminals with a facia having the necessary switches, MCB's, terminals etc. installed with the power circuit drawing, as given in Fig. IERL_ZSI implanted on it. Proper rugged holding brackets should be provided for moving the converter setup conveniently.

(15)The layout should be so designed to have as small stray inductances as possible, employing sandwiched busbars, as and where applicable.

(16) A warranty of 1 year has to be provided by the vendor for the components supplied by him (other than the components which the customer will provide to the vendor).

NOTE: An engineering write up must be provided by the vendor, while submitting the offer, (i) detailing how the FPGA digital I/O signals will be finally interfaced to the selected/designed gate drivers (ii) detailing how the 'desat' protection and 'dead time' feature of the selected reputed driver will be disabled (iii) giving a layout installation diagram of the major devices and components inside the converter (iv) giving the approximate size and weight of the enclosed setup.

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